J.M. LARAIA*
A.L.P. JANZON**
L.O.F. GONÇALVES***

SUMARIO

Este trabalho descreve um circuito digital de deteção multifrequencial, próprio para o reconhecimento de tons em Sistemas PCM. O dispositivo emprega um algoritmo inédito, baseado em transformada discreta de Fourier, e é implementado com tecnologia NMOS de 4 um, com porta de silício.

ABSTRACT

A digital multifrequency detector chip suitable for tone recognition in PCM systems   is described. It uses a novel algorithm based on discrete Fourier transform and is implemen ted in 4 um Si-gate NMOS.

* Engenheiro eletrônico (ITA-1979); especificação e projeto de circuitos integrados; Vér tice Sistemas Integrados, R. Carlos Guimarães 248/102, Campinas - SP, CEP 13100, tel. 51 -2366.

** Engenheiro elétrico (UNICAMP - 1978); especificação e projeto de circuitos integrados; Elebra Microeletrônica, R. Bogaert 326, V. Vermelha, São Paulo - SP.

*** (Ver outro trabalho de autoria de Luiz Otávio Fontenelle Gonçalves)

A well-known problem in many communication systems is how to execute the   detection of
tones, or in other words, how to decide whether or not during a certain time interval a
specific frequency has been received.

It was not until the mid-seventies that the availabity of inexpensive memories   enable
filtering to be performed by mathematical calculation, offering an alternative to   the
passive and active filters used as the only resource to the date. With the pressures of
futher reducing costs, new algorithms were proposed in order to save hardware, employing
techniques such as correlation, zero-crossing count and fast Fourier transform.

In this decade, with the advancements of integrated circuit technology and greater densi
ties of components made possible on the silicon, there is a definite trend towards the
integration of whole systems in a single chip. In the analog field this resulted   among
other products in complete banks of filters integrated using switched-capacitor   techni
ques. But the most remarkable advances occured with the digital circuits. One of   the
great advantages of the digital approach is that the same hardware may be designed to
perform effectively a large variety of functions. Thus, the need of a wide range of a-
pplication and real-time processing capabilities has led to the creation of commercial
"single-chip" digital signal processors (DSP's) as a family og components which combine
general purpose architecture and number-crunching hardware. However, there is a penalty
in power consumption, cost and package size that could be avoided in most applications by
a component tailored to execute more specific functions. With an architecture   oriented
to perform an otimized algorithm, it is frequently possible to get a much more efficient
component, or even to make feasible functions not covered by state-of-the-art comercial
DSP's.

The custom DSP implementation described in this paper, although primarily designed for
a multifrequency cod (MFC) signaling receiver used in a digital exchange, is   sufficien
tly versatile to be employed in a number of applications envolving detection of frequen
cies in PCM systems.

SPECIFICATIONS

The R2 signaling specifications that are important to the design are sumarized   below :
the dual tone signal consists of the linear addition of two voice frequency signals.Both
are selected from either a group of frequencies called the "High Group", or from another
group called the "Low Group", depending whether the exchange in question is the origina
tor or the receiver the communication. Each group has six frequencies, as shown in Table
1.

	High Group	Low Group
1	1380 Hz	1140 Hz
2	1500 Hz	1020 Hz
3	1620 Hz	900 Hz
4	1740 Hz	780 Hz
5	1860 Hz	660 Hz
6	1980 Hz	540 Hz

Tabela 1 - R2 signaling frequencies

The detector should recognize signals with deviation up to $\pm$ 10 Hz and reject any signal with deviation greater than $\pm$ 60 Hz. The required dynamic range is 30 dB. If the amplitude of each signal do not differ by more than 5 dB for adjacent frequencies, or 7 dB for non-adjacent frequencies, detection of both signals is madatory. If one amplitude is more than 20 dB below the other one, then the correspondent signal should not be recogni zed.

Signals lasting less than 7 ms should be rejected and time spent to detect a signal plus the time needed ot detect its end must not total more than 80 ms. The allowed signal to noise ratio is 20 dB.

DESIGN APPROACH

The input signal used for the algorithm development is a sequence of n instantaneous sam ples of a cosinusoidal wave with radian frequency ω, unitary amplitude and initial phase θ. This signal is represented by a function of time defined below, parameterised in ω, θ and n:

$$g_{\omega,\theta,n}(t) = \sum_{i=1}^{n} \delta(t-iT) \cos(\omega t+\theta) \qquad (1)$$

where $\delta(t)$ is the Dirac delta function. The Fourier transform of $g_{\omega,\theta,n}(t)$ in the frequency f_D is given by:

$$\hat{g}_{\omega,\theta,n}(f_D) = \int_{-\infty}^{\infty} g_{\omega,\theta,n}(t) \, e^{-j\omega_D t} \, dt =$$

$$= \sum_{i=1}^{n} |\cos(\omega iT +\theta)| \, e^{-j\omega_D iT} \qquad (2)$$

Based on some properties of equation (2), it was theoretically developed an adaptive algorithm which presents some very desirable characteristics for tone detection, including:

- wide dynamic range
- low false detection rate
- operation with poor signal-to-noise ratio
- capability of detecting superposed signals
- insensitivity to signal phase
- good immunity to harmonic and intermodulation distortion
- low sensitivity to rounding errors
- easy digital implementation

An extensive work of simulation confirmed these characteristics and was useful to optimi ze the algorithm, choosing the most adequate constants in order to obtain better performance and minimize the hardware. Simulation results for a situation where there are two tones and white gaussian noise present in the input signal, can be seen in Figure 1.

Precision is relaxed wherever possible in order to save hardware, but simulations have shown that the overall effect in performance is negligible because of the intrinsic algo rithm properties. One of the approximations in done with the amplitude of a quadrature pair. The digital implementation of the relation (3) is done very easili with the crude approximation (4):

$$Z = \sqrt{x^2 + y^2} \qquad\qquad (3)$$

$$Z' = |x| + |x| \qquad\qquad (4)$$

The incoming PCM data has to be internally linearized. If it were maintained the full PCM resolution, the linearized samples should have 12 bits, including the signal bit. However there is a rounding and the 3 least significant bits are eliminated, saving three sets of arithmetic cells and data buses. Dynamic range is still kept in excess of 40 dB.

For the circuit operation a sequence of sine and cosine samples of each detection frequence must be supplied by a external ROM. These samples are hardlimited to a three-level representation, as shown in Figure 2.

That can be expressed in harmonic series by the equation (5):

$$f(\omega t) = \frac{2\sqrt{3}}{\pi} \left(\cos \omega t - \frac{\cos 5\omega t}{5} - \frac{\cos 7 \omega t}{7} + \frac{\cos 11 \omega t}{11} + \ldots \right) \qquad (5)$$

It should be noted that the third harmonic is not present, and the fifth harmonic ampli-
tude is 14 dB below the fundamental component. This is important to guarantee   that
signals containing frequencies that are submultiple of the detection frequency   do not
wrongly activate the detector, because of the aliasing.

The trigonometric samples have to be multiplied by the converted PCM input. Its two-bit
quantization makes possible to accomplish this operation with a simple 8 x 2 multiplier.

IMPLEMENTATION

Once the algorithm and a compatible technology have been chosen, the architecture   has
come as a space x time trade-off. The serial design approach allows smaller chip   size,
while the parallel techniques usually imply greater area on the chip,   and   consequent
higher power dissipation, but yields higher speed and easier control.

The algorithm was tested in a breadboard and needed about 50 TTL IC's, among   MSI   and
and SSI parts. In an attempt to convert the TTL design to an NMOS one, several alterna-
tives had to be considered. The final design involved the use of a 16-bit parallel pro-
cessor to meet the speed constraints for the real-time process. Even though   the   data
buses are 16-bit wide, the chip does not occupy a large amount of area, because of two
main reasons: the care taken during the algorithm definition and logic mininization, and
the strategy of using metal control lines crossing perpendicularly short poly data buses,
embebded in handcrafted cells with standard height matching the RAM I/O pitch. This last
feature allows a surprisingly compact and efficient layout of the arithmetic block.

The final architecture exhibited a highly planar topography, and there   are   no inter-
connection lines that cross each other. This led to a remarkably regular   and modular
layout.

As shown in Figure 3, the chip has a serial-to-parallel input register, connected to an
128 x 8 bit ROM that performs the PCM A-law to linear conversion. μ-law conversion   is
possible with a change int the programming mask. The ROM interfaces with the arithmetic
block, which receives also the trigonometric samples. The output is transmitted through
an 8-bit serial register. The control block is synchronized by external clock   signals
and has the function of keeping the aritmetic block performing its functions   in   the
correct sequence. It is composed of a 16-bit adder and combinational circuitry. Although
the overall control can not be presented here in detail, a two-phase clock was utilized
and the timing of the process is sketched in Figure 4, where it is shown the   division
of the PCM sampling interval in 8 time slots. One detection frequency is processed   in
each one of the last seven time slots, while the first one is reserved for common   cal-
culations. Internally the slots are subdivided in 16 cycles,   each having   2   clock

periods. It is the cycle decoding that effectively comands the sequence of arithmetic
operations.

In the arithmetic block (Figure 5) the data are represented in two's complement notation.
The 16-bit data buses are shared by two registers, an adder, an 8 x 2-bit multiplier, a
module extractor, a magnitude comparator and a 26-word RAM. Considering the cyclic
chacarteristics of the process and the fixed clock rate, it was selected a dynamic RAM
with three transistors per cell. An equal output was added to the comparator, improving
the circuit visibility and making easier the design of the test pattern. The whole block
occupies approximately half of the total chip area.

The chip layout was totally handcrafted whit the aid of a symbolic layout editor.

PERFORMANCE AND APPLICATIONS

For the circuit implementation it is used a 4 micron silicon gate NMOS technology, with
depletion load transistors and single layers of metal and polysilicon.

Table 2 sumarizes the basic hardware characteristics of the digital detector. The micro
photograph can be seen in Figure 6.

Originally the algorithm and circuit were conceived to meet the R2 interregister sig-
naling system. On the other hand, as those specifications are relatively stringent, and
the chip interface and internal structure were designed with the necessary flexibility ,
it is expected that the detector should work without problems under other signaling sys
tems, such as R1, N⍛ 5, Socotel and DTMF (Touch-Tone [R]).

Package	18-pin DIP
Chip size	3.0 x 2.8mm
Number of transistors	5500
Power sypply	5 volt (single)
Power consumption	50 mW (typical)
I/O interface	TTL compatible
Technology	4 μm Si gate NMOS

Table 2 - Hardware Characteristics

Up to seven independent frequencies in the voiceband may be programmed simultaneously for
detection, using an external ROM with a sequence of sine and cosine sample of each fre-
quency. However, it is recommended for practical reasons that the resolution is set   at
a convenient value, limiting the number of samples. The number of sampling points needed
for each detection frequency is given by (6):

$$n = \frac{f_s}{R} \qquad\qquad (6)$$

where: n = number of sampling points

      f_s = sampling frequency (Hz)

      R = detector resolution (Hz)

If f_s is an exact multiple of R, the last sample will coincide with the first one and it will be supplied a continuous sampling of the detection frequency, what is desirable for good operation. An adequate resolution value is 20 Hz, that will demand 400 sampling points in a PCM system sampled at 8 kHz. Taking advantage of the simetry properties of the sinusoidal function with very little extra hardware, it is possible in this case to use 100 x 4 bits of external memory for each frequency.

In the Table 3 there is a sumary of the basic performance characteristics of a signalling receiver based on the described chip.

Sampling rate	8 kHz
Clock rate	2.048 MHz
Detection range	0 to 4000 Hz
Approximate bandwidth	70 Hz
Output refresh interval	25 ms

Table 3 - Performance characteristics
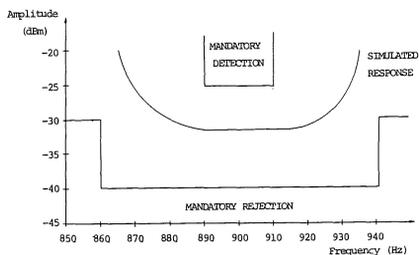
ACKNOWLEDGEMENTS

Fig. 1   Simulated response for 900 Hz detector
with fixed 780 Hz tone at − 20 dBm and
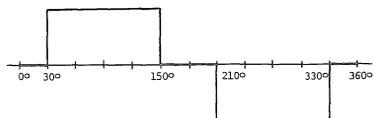white gaussian noise at − 40 dBm.
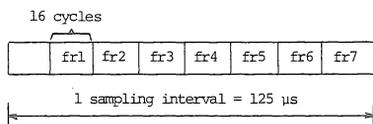

Fig. 2   Sine/cosine quantization.
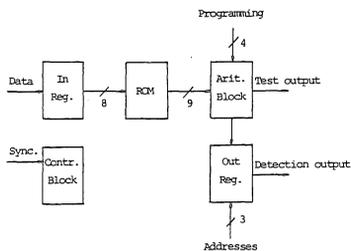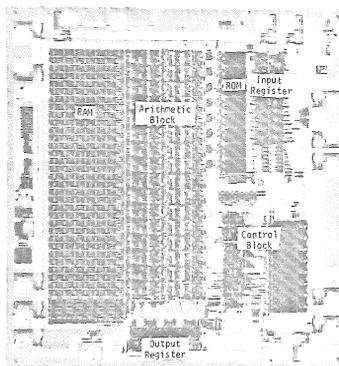

Fig. 4   Internal timing.

Fig. 3   Block diagram.

Fig. 6   Microphotograph of the digital detector